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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,073	12/23/2003	Takashi Ichimori	2003-1815A	7424
513	7590	01/04/2006	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021			MONDT, JOHANNES P	
		ART UNIT	PAPER NUMBER	3663
DATE MAILED: 01/04/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/743,073	ICHIMORI, TAKASHI
	Examiner	Art Unit
	Johannes P. Mondt	3663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 08 November 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-4 and 7-13 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4 and 7-13 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination ("RCE") under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/08/2005 has been entered.

Response to Amendment

Amendment filed 11/08/2005 with said RCE forms the basis for this office action. In said Amendment Applicant cancelled claims 5 and 6 (claims 14-20 had previously been cancelled) and substantially amended claims 1-4 and 7-13. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claims 1-4 and 7-13*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the

time the application was filed, had possession of the claimed invention. In particular, the only embodiment disclosing a hard mask is the first, and is illustrated by Figures 1-6. However, the second etching step, in which said lower electrode and said contact film are etched to expose the substrate is not performed "in a self-alignment manner with said hard mask" as recited in claim 1, line 14, but instead in a self-alignment manner with said first cover film 20, as clearly shown by Figure 4: not the hard mask but the cover film determines the boundary of the etched region.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. ***Claims 1, 4, 8, 9, 10, 12 and 13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al (US 2002/0074601 A1) in view of the Prior Art as Admitted by Applicant, or, in the alternative, in view of Kanaya et al (6,611,014 B1). *Fox et al teach a method of manufacturing a ferroelectric device* (see title) comprising steps of: providing a substrate 100 on IC circuit wafer (hence semiconductor substrate)(par. [0039]);

forming a multi-layer body by depositing successively a contact film 102 ([0038]), a lower electrode 104 ([0039]), a ferroelectric film 106/108 ([0040]) and an upper

electrode 110 ([0044]) on said substrate; and processing said multi-layer body (steps 300 and 404; see Figure 4 and [0053]-[0056]), wherein said processing step comprises: etching (step 300) said upper electrode and said ferroelectric film (Figure 4 and [0053]);

heat treatment (step 402: Figure 4 and [0055]; see also the equivalent step 208 as described in [0041]) said ferroelectric film in an oxidizing atmosphere ([0015]) under a condition wherein said contact film is covered with said lower electrode;

forming (step 400) a first cover film 112 so as to cover side surfaces of said upper electrode 110 and said ferroelectric film 106/108; and etching (step 404; Figure 4 and [0056]) said lower electrode.

Fox et al do not necessarily teach the further limitations (a) that said second etching step is carried out in a self-alignment manner with a hard mask on top of the upper electrode and also etches said contact film 102, thereby exposing said insulating substrate 100, (b) that said hard mask is formed on said upper electrode as an etching stopper. However, ad (a) it would have been obvious to include said further limitation in view of in view of Kanaya et al, who teach the second step to etch also the contact film 301 while the etching step is carried out in a self-alignment manner (col. 8, l. 42-58, col. 10, l. 60-67 and col. 11, l. 60-64: it is noted that the hydrogen barrier layer, be it 101 or 301, is an adhesive layer and thus meets the definition of contact layer in the Specification, page 4) with (ad (b)) a hard mask (104, 204, 304, e.g.; see, for instance Figure 15) formed on said upper electrode. Motivation to include the teaching by the

Prior Art as Admitted by Applicant, or, in the alternative, the teaching by Kanaya et al on the contact layer at least derives from the function of said contact layer, as a layer to make contact with the lower electrode: in the locations where said lower electrode is absent there also is no need for said contact layer. Thus a more functionally focused device is achieved. Furthermore, self-alignment has long been recognized as a reliable manner of ensuring accurate lateral positioning of layers relative to each other, - obviously crucial to any high-density integrated circuit capacitor structure such as the invention by Fox et al as any additional separate alignment step becomes more difficult with decreasing spatial scales.

On claim 4: said method by Fox et al includes etching said first cover film together with said multi-layer body (Figure 4 and [0056]).

On claim 8: the method by Fox et al further comprises a step 218 for forming a second cover film 112 ([0049] and [0056] and Figure 4) so as to cover said multi-layer body after said etching of said lower electrode and contact film.

On claim 9: the method by Fox et al further comprises heat treating (step 406) ([0056] and Figure 4) said ferroelectric film after said second cover film.

On claim 10: the contact film 102 of the method by Fox et al includes a binding film 102 ([0038] and Figure 4).

On claim 12: said heat treating in Fox et al is performed to recover a crystalline structure in the ferroelectric film ([0041], [0051] and [0055]).

On claim 13: said heat treating of said ferroelectric film in Fox et al and as claimed here in claim 9 is performed to recover a crystalline structure in the ferroelectric

film after said forming of the second cover film ([0016])(step 502: see [0060] and Figures 4-5); see also the patent cited and incorporated by reference in Fox et al in this regard), while furthermore the additional heat treatment (anneal) inherently causes further crystallization unless crystallization is perfect to start with, which obviously is not expected by overwhelming probability against it.

3. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and Kanaya et al as applied to claim 1 above, and further in view of Jung et al (JP 2001-044377, IDS item AJ). *Fox et al teach an insulating film (titanium oxide) 100 disposed on said substrate that is a semiconductor substrate having a transistor ([0038]) (i.e., "CMOS integrated circuit wafer"). Fox et al do not necessarily teach the further limitation that a contact plug to be formed so as to electrically connect said transistor to said contact film. However, it would have been obvious to include said further limitation in view of Jung et al*, who, in a patent publication on a ferroelectric capacitor for a transistor, hence analogous art, teach a contact plug 114 formed so as to pass through said insulating film 108/112 and electrically connect the transistor (with gate 104 and source/drain regions 106) with said contact film (through its un-etched sides). *Motivation* to include the teaching in this regard by Jung et al in the invention by Fox et al derives from the obvious applicability of the invention by Fox to those FRAM embodiments wherein the electrical connection between the drain region of the transistors of the CMOS integrated circuit and the ferroelectric capacitor is achieved through the insulating substrate over the CMOS wafer, i.e., through the shortest route possible, thus saving ohmic dissipation and material investment.

4. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and Kanaya et al as applied to claim 1 above, and further in view of Prior Art as Admitted by Applicant. As detailed above, claim 1 is unpatentable over Fox et al in view of Kanaya et al. Furthermore, in the first etching step in the Prior Art as Admitted by Applicant the lower electrode is partly etched in said etching of said upper electrode and said ferroelectric film so as to arrive at a predetermined thickness of the lower electrode. *Motivation* to include the teaching in this regard by Prior Art as Admitted by Applicant at least derives from the implied means to set the thickness of the lower electrode.

5. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and Kanaya et al as applied to claim 4 above, and further in view of Ohyagi (US 2003/0211685 A1). Although neither Fox et al nor Kanaya et al necessarily teach the further limitation defined by claim 7, it would have been obvious to include said further limitation in view of Ohyagi, who, in a patent application drawn to a FeRAM device (title, abstract and [0003]), hence analogous art, teach to use resist as mask pattern for an etching step so as not to etch more than the area selected for etching (see [0023]). *Motivation* to include the teaching by Ohyagi in the invention by Fox et al derives from the need to accurately select a particular surface area for etching.

6. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al and Kanaya et al as applied to claim 10 above, and further in view of Nagano et al (US 2002/0195633 A1). As detailed above claim 10 is unpatentable over Fox et al in view of Kanaya et al. Neither Fox et al, nor Kanaya et al necessarily teach the further limitation of the contact film to include an oxidation barrier film. *However, it would have*

been obvious to include said further limitation in view of Nagano et al, who, in a patent on a ferroelectric capacitor for a semiconductor memory device (title, abstract, [0004], [0104]), - hence analogous art, teach the inclusion of an iridium oxide (IrO₂) oxygen barrier film 31, as well as an iridium (Ir) oxygen barrier film between a platinum (Pt) lower electrode and the substrate so as to prevent the cross-layer diffusion of oxygen (Figure 1B, abstract, [0013] and [0103]). Motivation to include the teaching in this regard by Nagano et al in the invention by Fox et al derives from the deleterious effect of oxygen diffusion to contact plugs in ferroelectric capacitor semiconductor devices. The teaching can be combined with the invention because the material constitution of the layers (oxide substrate 45 ([0179]), platinum lower electrode 31d ([0103]) and lead zirconate titanate (PZT) (inter alia) ([0185]) and the generally metallic constitution of the contact plug to be protected against oxidation, imply the same conditions for oxygen diffusion, thus requiring the same measures.

Response to Arguments

Applicant's arguments filed 11/08/2005 have been fully considered but they are not persuasive. In particular, the step of etching the lower electrode has not been disclosed to be carried out in a self-alignment manner with said hard mask 19, because as is evident from Figures 1-6 (embodiment with hard mask (19)) and the related discussion ([0020]-[0031]) the second etching step is carried out with cover film 20 determining the self-alignment process (see specifically Figure 4 and [0027]). Therefore,

the limitation "etching, in a self-alignment manner with said hard mask" forms new matter.

Furthermore, the substantial amendment to claim 1 only introduces limitation that are obvious over the prior art already cited. See first cover film 112 and related etching step in Figure 5, and please note the final structure is achieved topographically at the end of said etching step 500 (annealing does not change the topography). Self-alignment has long been recognized in the art of semiconductor memory integrated circuits as particularly advantageous because of the ever-increasing device density, because with device density the alignment of capacitor layers becomes more difficult to achieve. Finally, both self-alignment and a hard mask topping and protecting the upper electrode are taught by the secondary reference, Kanaya et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
December 23, 2005

Patent Examiner:



Johannes Mondt (Art Unit: 3663).